## TUTORIAL: Quick Start Undertow Suite

Thank you for your interest in our Undertow Suite product. There are several ways to initiate the program with your simulation files:

**Example 1:** The command for users running a simulator in batch mode.

% ut -iv -f FMS/top.vc -sigfile FSM/fsm.sigs

- 'ut' is used to start the Waveform window
- '-iv' is used to start up the source code debugger
- '-f' indicates that the next argument is a filename that contains all of your design files (In this case these are Verilog files listed in the top.vc file)
- '-sigfile' indicates that the next argument is the name of your signal file

**Example 2:** The command for users running an interpreted simulator interactively. In this case we will run the Verilog XL simulator:

% ut -iv -xl verilog -f FMS/top.vc -sigfile FSM/fsm.sigs -tracefile FSM/fsm.trace

- '-xl verilog' indicates the type and name of the simulator
- '-tracefile' indicates that the next argument is the name of the trace file

NOTE: Loading a trace file will allow the Undertow Suite to act just like a real simulator without tying up a simulator license. This is the feature called 'Virtual Simulation'.

**Example 3:** The command for users running a compiled simulator interactively. In this case we will run the Synopsis VCS simulator:

% ut -iv -vcs vcs top -sigfile FSM/fsm.sigs -ivsimcmp "-f FSM/source"

- '-vcs vcs' indicates the type and name of the simulator
- 'top' is the file name of the compiled design
- '-ivsimcmp' indicates the files that were previously compiled by the simulator

NOTE: To build a parsed database for debugging the source code, Undertow Suite needs the file names of the previously simulation compiled files.



## Thanks for the opportunity to serve you.

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